Release note [version v.1.0.0]

1. History

Release v.1.0.0

> **[v.1.0.0] First release [*details*]**

New repository architecture

> **[v.0.11.0] Change of the repository architecture [*details*] :**
>
> - LpGBT-FPGA repository contains only the VHDL modules used to implement the IP
> - Remove the simulation testbench (example design)
> - Creation of a new repository for the simulation testbench: https://gitlab.cern.ch/gbt-fpga/lbgbt-fpga-simulation

Documentation: README file

> **[v.0.7.0] Improves README.md (documentation) [*details*]**
>
> **[v.0.7.5] Improves README.md (fix documentation link issue) [*details*]**
>
> **[v.0.7.9] Improves README.md (warns about new philosophy) [*details*]**
>
> **[v.0.9.0] Update README file (correction from Sophie B.) [*details*]**
>
> **[v.0.9.1] Update README file (correction from Sophie B.) [*details*]**

Bug fix

> **[v.0.10.0] Fix ByPass issue [*details*] :**
>
> - Bus size didn't match when FEC bypass was selected (uplink)

Add SerDes interface and Doxygen comments

> **[v.0.5.0] Add serial link [*details*] :**
>
> - Implementation of MGT emulation
> - Add Tx and Rx gearboxes with oversampling (configurable)
> - Add pattern search module (configurable)
> - Re-organize repository
> - Improve CI scripts (test lost of lock)
>
> **[v.0.5.1] Fix CI compilation issue (1/2) [*details*] :**
>
> - Delete rxGearbox.vhd

[v.0.5.2] Fix CI compilation issue (1/2) [*details*] :

- Add rxgearbox.vhd (change from upper to lower case)

[v.0.5.3] Fix CI simulation issue [*details*] :

- Fix signal force issue (format from hexa to integer - linux issue)

[v.0.6.0] Doxygen comment and decoder duplication @5.12Gbps (dynamic mode) [*details*] :

- Use the upper side of the frame to decode second phase in dynamic mode @5.12Gbps
- Comment the datapath sources for doxygen

[v.0.6.1] Fix decoder and de-interleaver issue [*details*]

[v.0.6.2] Add comments for doxygen [*details*]

[v.0.7.9] Improves README.md (warns about new philosophy) [*details*]

[v.0.8.1] Bug fix and cleaning [*details*] :

- Rename mgt*pattsearch to mgt*frameAligner
- Rename RS encoder in RS decoder (uplink decoders)
- Fix CI bug (RxPMA offset init)
- Fix compilation issue in frameAligner module (signal not declared)

Continuous integration

[v.0.3.0] Continuous integration [*details*] :

- Add continuous integration scripts

[v.0.3.1] Update CI scripts [*details*] :

- Fix source issue
- Add quit with error if simulation fails

[v.0.3.2] Update CI scripts [*details*] :

- Fix filename/path issue in testbench.tcl (linux)

[v.0.3.3] Update CI scripts [*details*] :

- Fix filename/path issue (wrong name)
- Fix signal force issue (linux/questa)

[v.0.3.5] Update CI scripts [*details*] :

- Add return value to compile_project function (0 in case of success)

[v.0.3.6] Update CI scripts [*details*] :

- Set work/ as a cached folder (used by questa for the simulation)

[v.0.3.7] Update CI scripts [*details*] :

- Add reset_wave call to create waveform artifact

[v.0.3.8] Update CI scripts [*details*] :

- Add downlink test

[v.0.3.9] Test CI scripts [*details*] :

- Add errors in interleaver/deinterleaver modules (jobs shall fail)

[v.0.4.0] Ready to use [*details*] :

- CI scripts successfully tested
- Uplink and downlink paths successfully tested

Add downlink and uplink datapath logic

[v.0.1.0] Downlink datapath [*details*] :

- Add LpGBT-FPGA files for the downlink datapath
- Add LpGBT model (downlink datapath only)
- Add TCL file to run the simulation
- Add Testbench top level that connects the LpGBT-FGPA downlink datapath to the LpGBT ASIC model
- Update README.md

[v.0.2.0] Uplink datapath [*details*] :

- Add LpGBT-FPGA files for the uplink datapath
- Add LpGBT model (uplink datapath)
- Update repo architecture
- Add scripts to automatically validate the IP (simulation)

2. Files

Following files have been added/modified/removed since the last release [version v.0.0.1]:

- File: README.md with **126 additions** and **4 deletions**
- File: dataPath/downlink_dataPath.vhd with **160 additions** and **0 deletions**
- File: dataPath/downlink_fecEncoder.vhd with **98 additions** and **0 deletions**
- File: dataPath/downlink_interleaver.vhd with **107 additions** and **0 deletions**
- File: dataPath/uplink_dataPath.vhd with **282 additions** and **0 deletions**
- File: dataPath/uplink_decoder.vhd with **273 additions** and **0 deletions**
- File: dataPath/uplink_deinterleaver.vhd with **130 additions** and **0 deletions**
- File: dataPath/uplink_deinterleaverFec12.vhd with **236 additions** and **0 deletions**
- File: dataPath/uplink_deinterleaverFec5.vhd with **141 additions** and **0 deletions**
- File: dataPath/uplink_descrambler.vhd with **263 additions** and **0 deletions**
- File: fecCodec/fec_rsDecoderN15K13.vhd with **277 additions** and **0 deletions**
- File: fecCodec/fec_rsDecoderN31K29.vhd with **457 additions** and **0 deletions**
- File: fecCodec/fec_rsEncoderN7K5.vhd with **108 additions** and **0 deletions**
- File: gearbox/rxgearbox.vhd with **126 additions** and **0 deletions**
- File: gearbox/txgearbox.vhd with **131 additions** and **0 deletions**
- File: lpgbtfpga_package.vhd with **23 additions** and **0 deletions**
- File: mgtFrameAligner/mgt_frameAligner.vhd with **292 additions** and **0 deletions**
- File: scrDscr/descrambler_51bitOrder49.vhd with **69 additions** and **0 deletions**
- File: scrDscr/descrambler_53bitOrder49.vhd with **69 additions** and **0 deletions**
- File: scrDscr/descrambler_58bitOrder58.vhd with **68 additions** and **0 deletions**
- File: scrDscr/descrambler_60bitOrder58.vhd with **69 additions** and **0 deletions**
- File: scrDscr/scrambler_36bitOrder36.vhd with **75 additions** and **0 deletions**